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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/701,884	Applicant(s) JEFFERSON ET AL.	
	Examiner Kevin Quinto	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10,12-21,23-26,29,30 and 32* is/are rejected.

7)☒ Claim(s) *8,11,22,27,28 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9, 10, and 12-21, 23-26, 29, 30, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kizuki (USPN 5,679,962) in view of Bestwick et al. (USPN 5,571,376) and further in view of Chapple-Sokol et al. (USPN 5,612,255) and further in view of Doyle et al. (USPN 6,063,688).

4. In reference to claims 1, 2, and 16-18, Bestwick et al. (USPN 5,571,376, hereinafter referred to as the "Bestwick" reference) discloses a similar device. Figure 3 of Bestwick illustrates a substantially one-dimensional elongate conducting means or a quantum wire structure. There is a first semiconductor (52) which is substantially surrounded by a second semiconductor (50). The elongate conducting means or quantum wire is provided within a groove in the second semiconductor (50). This groove is structured such that both walls of the groove are substantially planar surfaces

which are roughly parallel to crystal plane (111) on which the first semiconductor (52) is substantially zero. The first semiconductor (52) of Bestwick is GaAs (gallium arsenide) while the second semiconductor (50) is AlGaAs (aluminum gallium arsenide). The applicant has disclosed that GaAs has a slow growth rate on a (111) plane of AlGaAs (p.12, specification). Bestwick discloses that the second semiconductor or AlGaAs (18) is grown in the groove (or an intersection of two walls) which is etched in the (111) plane orientation (column 3, lines 19-34). The examiner believes that the AlGaAs (18) is also in the (111) plane and thus meets this limitation of the claim. Bestwick does not explicitly disclose the use of the quantum wire in a transistor structure. However this particular usage for a quantum wire is well known in the art. Chapple-Sokol et al. (USPN 5,612,255, hereinafter referred to as the "Chapple-Sokol" reference) discloses that quantum wire channels have high electron mobility (column 3, lines 10-16). It is also well known in the art that high electron mobility for a transistor channel is desired. Doyle et al. (USPN 6,063,688, hereinafter referred to as the "Doyle" reference) discloses that quantum wire channels have increased electron mobility which leads to a higher drain saturation current thereby increasing chip speeds (column 10, lines 65-67, and column 11, lines 1-7). Kizuki (USPN 5,679,962) discloses a prior art single electron transistor which has a one-dimensional channel (labeled "Quasi – 1DEG") in figures 17(a) and 17(b). In view of Chapple-Sokol and Doyle, it would be obvious to use the quantum wire of Bestwick as the channel of Kizuki so as to attain a device with a high electron mobility. The single electron transistor of Kizuki constructed in view of Bestwick, Chapple-Sokol, and Doyle, has a channel formed of a quantum wire which

extends between source and drain electrodes (figures 17(a) and 17(b) of Kizuki). There is at least one further electrode (the electrode labeled "Gate 1" in figures 17(a) and 17(b) of Kizuki).

5. In reference to claim 3, figure 3 of Bestwick shows that the first semiconductor (52) is provided in the groove or the intersection of two walls.

6. In reference to claim 4, figure 3 of Bestwick shows that the second semiconductor (50) is formed in a groove which is itself formed in a substrate (1). The second semiconductor (50) lines the sides of the groove.

7. In reference to claim 5, Bestwick discloses that the first semiconductor (52) and the substrate (1) are made of GaAs (column 3, line 6 and column 4, lines 39-40).

8. So far as understood in claim 6, figure 3 of Bestwick shows that an elongate region of the first semiconductor (52) is in a bottom region of a groove lined with the second semiconductor (50).

9. In reference to claim 7, the transistor of Kizuki constructed in view of Bestwick, Chapple-Sokol, and Doyle, has a groove (with a quantum wire) formed in a top portion of the mesa.

10. In reference to claim 9, the transistor of Kizuki constructed in view of Bestwick, Chapple-Sokol, and Doyle, has a channel formed of a quantum wire which extends between source and drain electrodes (figures 17(a) and 17(b) of Kizuki). Kizuki discloses that a quantum dot is produced in the channel (column 3, lines 4-7) or along a region of the conducting means.

11. In reference to claim 10, Kizuki discloses that applying a voltage to the at least one further electrode (labeled "Gate 1" in figures 17(a) and 17(b)) helps to provide confinement for the quantum dot (column 3, lines 4-7).

12. So far as understood in claim 12, Kizuki discloses that applying a voltage to the at least one further electrode (labeled "Gate 1" in figures 17(a) and 17(b)) and additional electrode (labeled "Gate 1" in figures 17(a) and 17(b)) provides confinement for the quantum dot (column 3, lines 4-7) thereby meeting the limitation where the electrodes "provide confinement in a third dimension for charge carriers within the conducting means, in which hard confinement in two dimensions holds charge carriers within the conducting means."

13. So far as understood in claim 13, the transistor of Kizuki constructed in view of Bestwick, Chapple-Sokol, and Doyle, has a channel formed of a quantum wire which extends between source and drain electrodes (figures 17(a) and 17(b) of Kizuki). Figure 1D of Kizuki shows that the at least one further electrode (labeled "Gate 1" in figures 17(a) and 17(b)) and additional electrode (labeled "Gate 1" in figures 17(a) and 17(b)) are transverse to the channel or quantum wire or conducting means.

14. In reference to claim 14, the device of Kizuki constructed in view of Bestwick, Chapple-Sokol, and Doyle has electrodes which are capable of causing a peak within the energy bands of the first semiconductor (52) of the quantum wire or conducting means.

15. In reference to claim 15, figure 3 of Bestwick shows that the conducting means has a crescent shaped cross section (17).

16. With regard to claims 19, 24-26, 29, 30 and 32, the method of building the device of Kizuki constructed in view of Bestwick, Chapple-Sokol, and Doyle meets the limitation of the claim.

17. In reference to claim 20, Bestwick discloses using an anisotropic etch (column 3, lines 19-34).

18. In reference to claims 21, Bestwick uses an n-type epilayer (50).

19. With regard to claim 23, Bestwick uses a p-doped region (52) on top of the n-type epilayer.

Allowable Subject Matter

20. Claim 8, 11, 22, 27, 28, and 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of a quantum field effect transistor with a quantum wire formed of a GaAs core surrounded by AlGaAs where there is a plurality of quantum dots formed along the wire.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
March 24, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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